AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings, of claims in this application.

1. (Currently Amended) A delay locked loop (DLL) comprising:

a basic clock generator for generating a plurality of basic clock signals which are each shifted by a predetermined phase in response to an external signal;

a mixer for generating a first clock signal and a second clock signal which is 90 degrees out-of-phase with the first clock signal, in response to the plurality of basic clock signals;

a clock buffer for generating a first internal clock signal in response to the first clock signal and a second internal clock signal in response to the second clock signal;

a first duty corrector for correcting a duty of the first internal clock signal and feeding an output of the first duty corrector back to the clock buffer;

a second duty corrector for correcting the duty of the second internal clock signal and feeding an output of the second duty corrector back to the clock buffer;

a phase detector for comparing and detecting phases of the external clock signal and the second internal clock signal; and

a digital-to-analog converter for controlling phase ranges of the first and second clock signals generated in the mixer in response to an output of the phase detector.

2. (Original) The DLL of claim 1, wherein the basic clock generator generates eight basic clock signals which are progressively shifted apart by 45 degrees.

3. (Original) The DLL of claim 1, wherein each of the plurality of basic clock signals generated by the basic clock generator are separated by the predetermined phase, the predetermined phase dividing equally into a phase of 360 degrees.

4. (Original) The DLL of claim 1, wherein the first and second duty correctors maintain the duties of the first and second internal clock signals at 50%.

5. (Original) A delay locked loop (DLL), comprising;

a first amplifier for receiving an external clock signal and converting the external clock signal to a clock signal having a small swing width SS-CLK;

a first duty corrector for correcting a duty of the clock signal having the small swing width and feeding back the corrected clock signal to the first amplifier;

a basic clock generator for generating a plurality of basic clock signals which are each shifted in response to the clock signal having the small swing width;

a mixer for generating a first clock signal and a second clock signal which is 90 degrees out-of-phase with the first clock signal, in response to the plurality of basic clock signals, the first clock signal and the second clock signal each having the small swing width;

a second amplifier for amplifying the small swing width of the first clock signal to a CMOS swing width;

a third amplifier for amplifying the small swing width of the second clock signal to the CMOS swing width;

a clock buffer for generating a first internal clock signal in response to an output of the second amplifier and a second internal clock signal in response to an output of the third amplifier;

a second duty corrector for correcting the duty of the first internal clock signal and feeding an output of the second duty corrector back to the second amplifier;

a third duty corrector for correcting the duty of the second internal clock signal and feeding an output of the third duty corrector back to the third amplifier;

an output replica for copying a load of an output path of the first internal clock signal to a second internal clock signal;

a phase detector for comparing and detecting phases of the external clock signal and the second internal clock signal; and

a digital-to-analog converter for controlling phase ranges of the first and second clock signals generated in the mixer in response to an output of the phase detector.

6. (Original) The DLL of claim 5, wherein the basic clock generator generates eight basic clock signals which are progressively shifted apart by 45 degrees.

7. (Original) The DLL of claim 5, wherein each of the plurality of basic clock signals generated by the basic clock generator are separated by the predetermined phase, the predetermined phase dividing into a phase of 360 degrees.

8. (Original) The DLL of claim 5, wherein the second and third duty correctors maintain the duties of the first and second internal clock signals at 50%.

9. (Original) The DLL of claim 6, wherein the phase ranges of the first and second clock signals comprise eight octants.

10. (Original) The DLL of claim 9, wherein each of the first and second mixers comprise:

a selector for generating select signals in response to an output of the digital-to-analog converter;

a first phase MUX for selecting phase ranges of the plurality of basic clock signals in response to the select signals and determining the phase ranges of the plurality of basic clock signals as the phase ranges of the first clock signal; and

a second phase MUX for selecting the phase ranges of the plurality of basic clock signals in response to the select signals and determining the phase ranges of the plurality of basic clock signals as the phase ranges of the second clock signal.

11. (Original) The DLL of claim 10, wherein the first and second phase MUXs each comprise differential amplifiers which receive the basic clock signals and inverse signal pairs of the plurality of basic clock signals and are enabled by the select signals.

12. (Original) The DLL of claim 9, wherein the second and third duty correctors maintain the duties of the first and second internal clock signals at 50%.

13. (Original) The DLL of claim 9, wherein the clock buffer comprises:

a first path having a first chain of serially connected inverters for receiving the first clock signal and outputting the first clock signal to the second duty corrector;

a second path having a second chain of serially connected inverters for receiving the first clock signal and outputting the first clock signal as the first internal clock signal;

a third path having a third chain of serially connected inverters for receiving the second clock signal and outputting the second clock signal as the second internal clock signal; and

a fourth path having a fourth chain of serially connected inverters for receiving the second clock signal and outputting the second clock signal to the third corrector.

14. (Currently Amended) A delay locked loop (DLL), comprising;

a basic clock generator for generating a plurality of basic clock signals which are each shifted in response to an external signal;

a first mixer for generating a first clock signal in response to the plurality of basic clock signals;

a second mixer for generating a second clock signal which is 90 degrees out-of-phase with the first clock signal in response to the plurality of basic clock signals;

a clock buffer for generating a first internal clock signal in response to the first clock signal and a second internal clock signal in response to the second clock signal and in consideration of a line load of the first internal clock signal;

a phase detector for comparing and detecting phases of the external clock signal and the second internal clock signal; and

a digital-to-analog converter for controlling phase ranges of the first and second clock signals generated in first and second mixers in response to an output of the phase detector.

15. (Original) The DLL of claim 14, wherein the basic clock generator generates eight basic clock signals which are progressively shifted apart by 45 degrees.

16. (Original) The DLL of claim 15, wherein the phase ranges of the first and second clock signals comprise eight octants.

17. (Original) The DLL of claim 14, wherein each of the plurality of basic clock signals generated by the basic clock generator are separated by the predetermined phase, the predetermined phase dividing equally into a phase of 360 degrees.

18. (Original) The DLL of claim 14, wherein each of the first and second mixers comprise:

a selector for generating select signals in response to an output of an the digital-to-analog converter;

a first phase MUX for selecting phase ranges of the plurality of basic clock signals in response to the select signals and determining the phase range of the plurality of basic clock signals as the phase ranges of the first clock signal; and

a second phase MUX for selecting the phase ranges of the plurality of basic clock signals in response to the select signals and determining the phase ranges of the plurality of basic clock signals as the phase ranges of the second clock signal.

19. (Original) The DLL of claim 18, wherein the first and second phase MUXs each comprise differential amplifiers which receive the plurality of basic clock signals and inverse signal pairs of the plurality of basic clock signals and are enabled by the select signals.

20. (Original) A delay locked loop (DLL), comprising:

a basic clock generator for generating a plurality of basic clock signals which are each shifted in response to an external clock signal;

a first mixer for generating a first clock signal in response to the plurality of basic clock signals;

a second mixer for generating a second clock signal which is 90 degrees out-of-phase with the first clock signal in response to the plurality of basic clock signals;

a clock buffer for generating a first internal clock signal in response to the first clock signal and a second internal clock signal in response to the second clock signal and in consideration of a line load of the first internal clock signal;

a first duty corrector for correcting the duty of the first internal clock signal and feeding an output of the first duty corrector back to the second amplifier;

a second duty corrector for correcting the duty of the second internal clock signal and feeding an output of the second duty corrector back to the third amplifier;

a phase detector for comparing and detecting phases of the external clock signal and the second internal clock signal; and

a digital-to-analog converter for controlling phase ranges of the first and second clock signals generated in the first and second mixers in response to an output of the phase detector.

21. (Original) The DLL of claim 20, wherein the basic clock generator generates eight basic clock signals which are progressively shifted apart by 45 degrees.

22. (Original) The DLL of claim 21, wherein the phase ranges of the first and second clock signals comprise eight octants.

23. (Original) The DLL of claim 20, wherein each of the plurality of basic clock signals generated by the basic clock generator are separated by the predetermined phase, the predetermined phase dividing equally into a phase of 360 degrees.

24. (Original) The DLL of claim 20,wherein each of the first and second mixers comprise:

a selector for generating select signals in response to an output of the digital-to-analog converter;

a first phase MUX for selecting phase ranges of the plurality of basic clock signals in response to the select signals and determining the phase ranges of the plurality of basic clock signals as the phase ranges of the first clock signal; and

a second phase MUX for selecting the phase ranges of the plurality of basic clock signals in response to the select signals and determining the phase ranges of the plurality of basic clock signals as the phase ranges of the second clock signal.

25. (Original) The DLL of claim 24, wherein the first and second phase MUXs each comprise differential amplifiers which receive the plurality of basic clock signals and inverse signal pairs of the plurality of basic clock signals and are enabled by the select signals.

26. (Original) The DLL of claim 20, wherein the first and second duty correctors maintain the duties of the first and second internal clock signals at 50%.

27. (Original) The DLL of claim 20, wherein the clock buffer comprises:

a first path having a first chain of serially connected inverters for receiving the first clock signal and outputting the first clock signal to the second duty corrector;

a second path having a second chain of serially connected inverters for receiving the first clock signal and outputting the first clock signal as the first internal clock signal;

a third path having a third chain of serially connected inverters for receiving the second clock signal and outputting the second clock signal as the second internal clock signal; and

a fourth path having a fourth chain of serially connected inverters for receiving the second clock signal and outputting the second clock signal to the third corrector.